CHIPS JOINT UNDERTAKING

Anton Chichkov

27/09/2024

EUROPEAN PARTNERSHIP

What is Chips Joint Undertaking?

Public-private partnership (PPP)

Partnerships between public authorities and industry intend to bring project results closer to the market and improve the link between research and societal growth. The PPPs are based on long term contracts that can take many different legal forms, from contractual partnerships to specific legal entities.

Joint undertaking (JU)

A Joint Undertaking is an institutionalized PPP with its own legal identity, with its own governance, budget etc.. The JUs are established by an EU regulation.

Chips JU

Chips JU was established in September, 2023, in an amendment to the Single Basic Act to implement the first pillar of the Chips Act and to continue the activities of its predecessors in the field of electronic components and systems (ECS). The Chips JU is a tri-partite partnership between the EC, the participating states and European industries; most of our actions are funded jointly and equally by these actors.

CHIPS ACT: ENTRY INTO FORCE, 21 SEPTEMBER 2023

SIGNATURES 13 SEPTEMBER, PUBLICATION 18 SEPTEMBER 2023

Roberta Metsola (European Parliament President)

José Manuel Albares Bueno (Council Presidency)

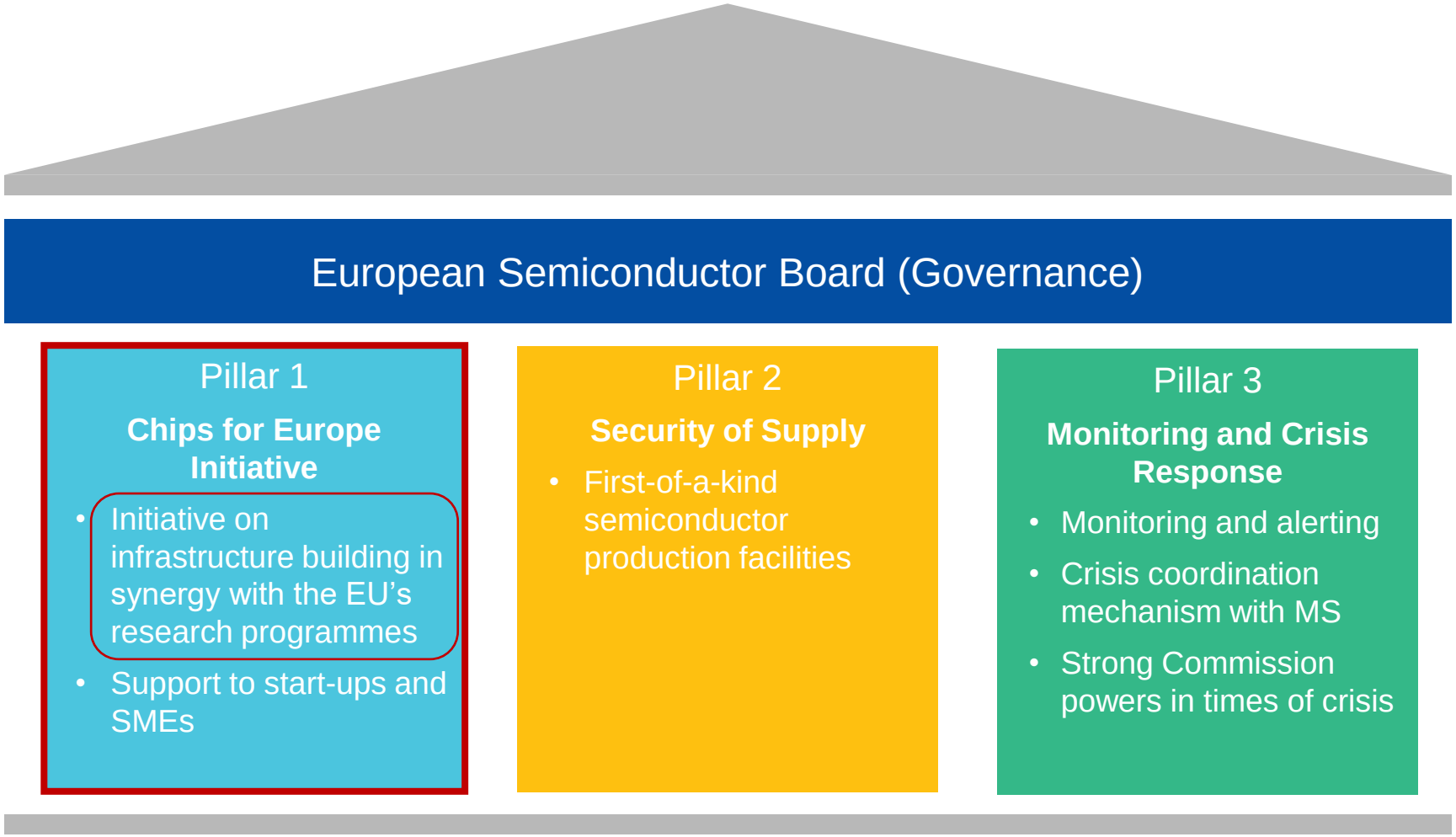
Chips Act:

https://eur-lex.europa.eu/eli/reg/2023/1781/oj

Single Basic Act amendment:

https://eur-lex.europa.eu/eli/reg/2023/1782/oj

THE 3 PILLARS OF THE CHIPS ACT



CHIPS JU AND ITS PREDECESSOR KEY DIGITAL TECHNOLOGIES JU (KDT JU)

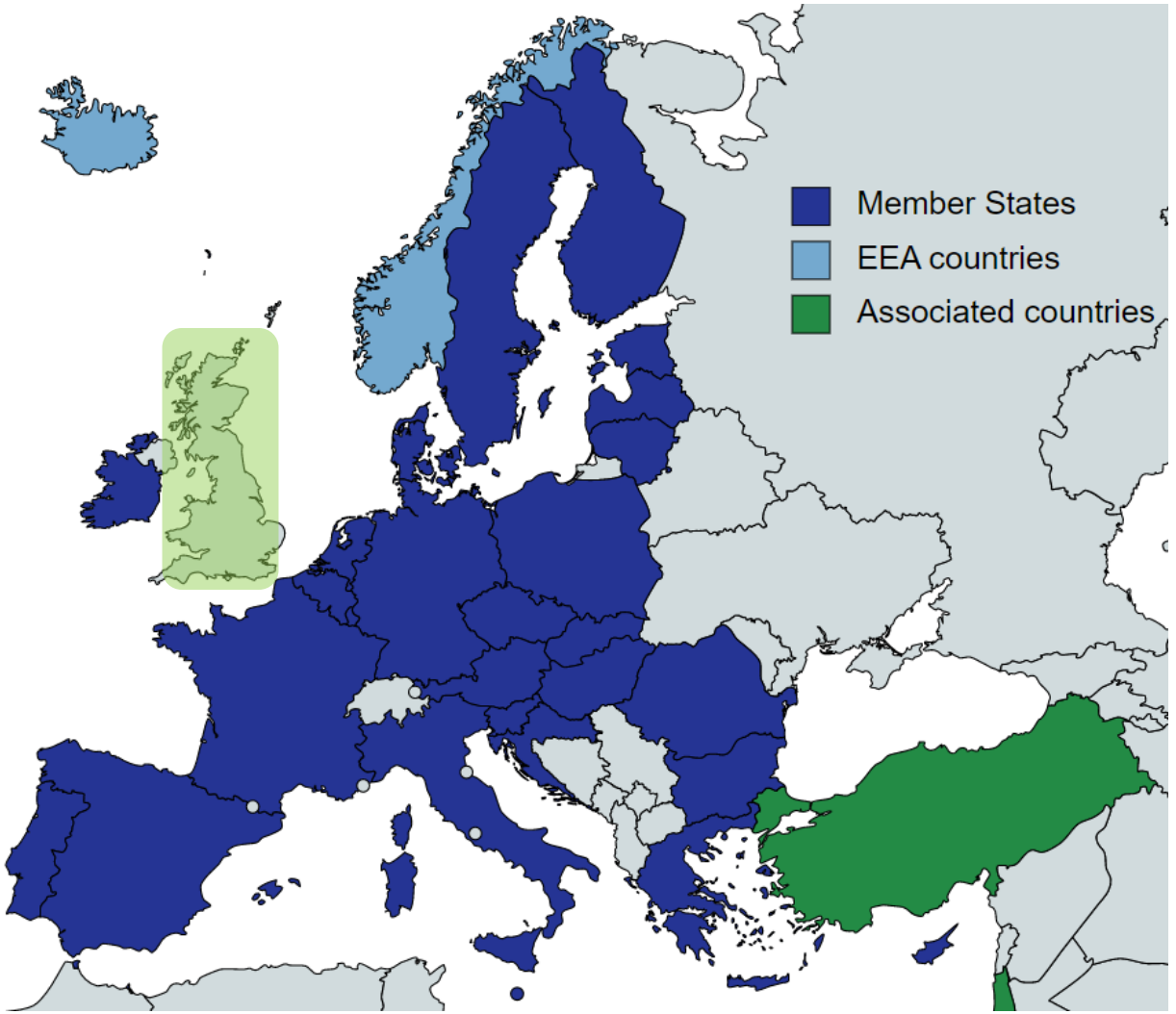
Non-initiative

- **KDT General Objectives**
  - a) Reinforce EU strategic autonomy in electronic components and systems
  - b) Establish EU scientific excellence and innovation leadership
  - c) Ensure that components and systems technologies address Europe's societal and environmental challenges
- **From KDT to Chips JU**
  - d) Pilot lines
  - e) Design platform
  - f) Competence centers
  - g) Quantum chips technology

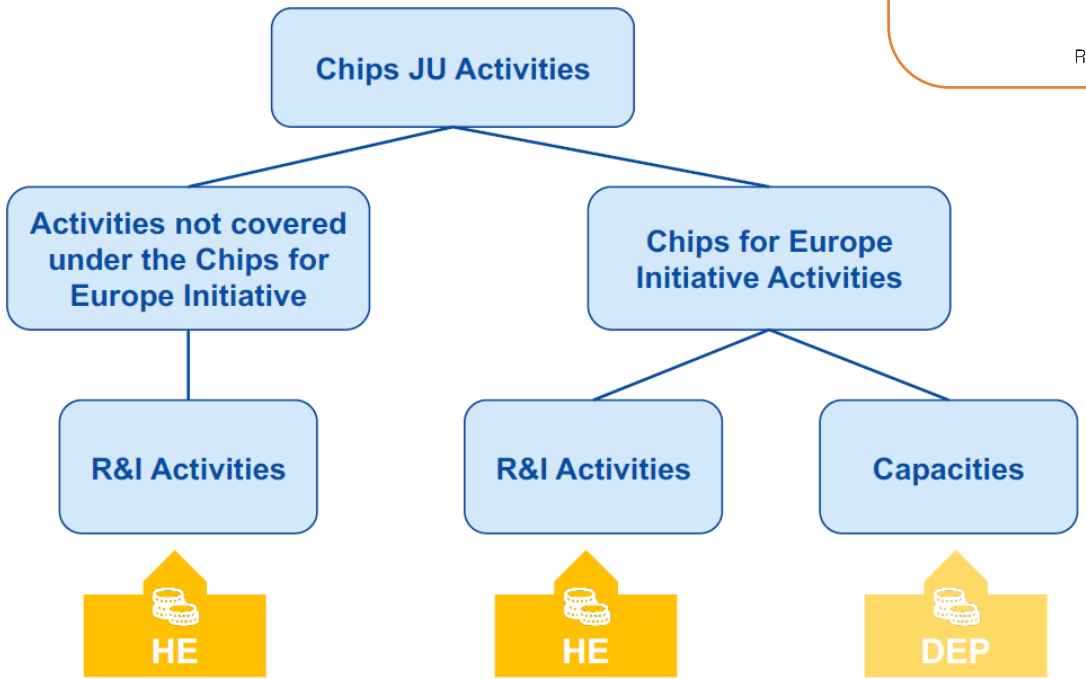
  Digital Europe Programme in addition to Horizon Europe

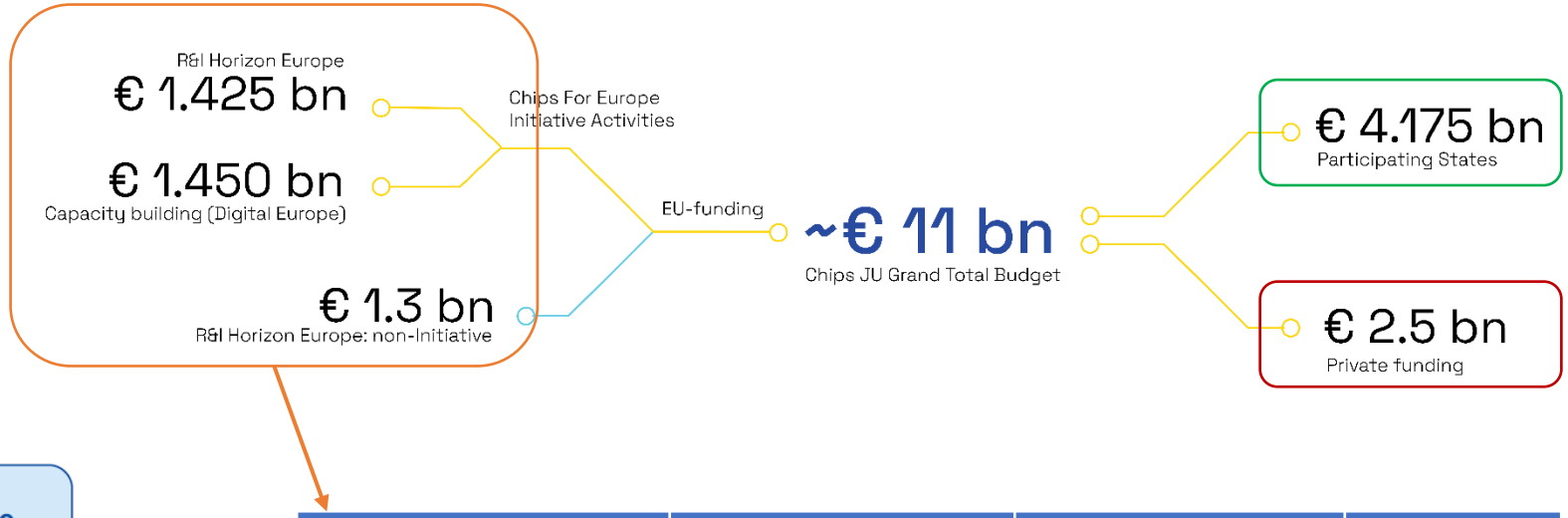
Initiative

- **Disclaimed:** ***we know that the WP2023-2027 will need to be updated/amended in the spring and some details on the following pages may change:***
  https://www.chips-ju.europa.eu/Library/
- How to participate:
  https://www.chips-ju.europa.eu/Participate/



CHIPS JU





EU Contribution to Chips JU (excl	Chips for Europe Initiative	Non-Initiative	Total
R&I (Horizon Europe)	1.425	1.300	2.725
Cap building (DEP)	1.450	n.a.	1.450
Total	**2.875**	**1.300**	**4.175**

CHIPS JU NONE INITIATIVE CALLS

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EUROPEAN PARTNERSHIP

CHIPS JU NONE INITIATIVE CALLS 2024

Action	Title	Maximum JU Funding (M€)
HORIZON-Chips 2024-1-IA-T1	Global IA call according to SRIA 2024	103.00
HORIZON-Chips 2024-1-IA-T2	Focus topic on “High Performance RISC-V Automotive Processors supporting SDV”	20.00
HORIZON-Chips 2024-1-IA-T3	Focus topic on “Service Oriented Framework for the Software Defined Vehicle of the future"	20.00
HORIZON- Chips 2024-2-RIA-T1	Global RIA call according to SRIA 2023	52.00
HORIZON- Chips 2024-2-RIA-T2	Focus topic on “Sustainable and greener manufacturing”	15.00
HORIZON- Chips 2024-3-RIA	Joint call with Korea on Heterogeneous integration and neuromorphic computing technologies for future semiconductor components and systems	6.00
		216.00

Chips JU IA proposals *(II Phase to Open)*

An IA proposal is characterized by:

- The activities have their centre of gravity at the **TRL 5-8.**
- Execution by **an industry led consortium**
- Developing **innovative technologies and/or using them in innovative ways**
- Establishment of a new and realistic innovation environment **connected with an industrial environment,** such as:
  - a pilot line facility capable of manufacturing
  - a zone of full-scale testing
  - a development of new processes or tools and their introduction in several domains
  - the development of frameworks or platforms together with the usage of these frameworks or platforms in innovative products.
- IA Prjects should contribute to, short to midterm **economic value creation** in Europe

Focus topic on High Performance RISC-V Automotive Processors Supporting SDV *(II Phase to Open)*

- RISC-V still requires important extensions and add-ons in order to support *high-performance automotive quality processing* needs.
  - Efforts should be focussed on the development of an **automotive RISC-V reference hardware platform**.
  - **Open-source RISC-V based hardware** system implementation of the **SDV Hardware Layer** compatible with one or multiple widely-agreed-upon **Hardware Abstraction Layers** of the vehicle of the future is targeted.
  - The expected RISC-V reference platform shall be targeted for **commercial use** and should comply with **industry standards** especially with respect to quality and safety.
  - It should contain all assets needed to enable the adoption of RISC-V cores throughout the European automotive ecosystem.

Focus topic on Software-define vehicle middleware and API framework for the vehicle of the future *(II Phase to Open)*

- Europe needs to join forces in order to lead on the Software Defined Vehicle (SDV) technology
- The SDV software stack should be extended by a **Middleware and Application Programming Interface (API) Framework**
  - **To** supports different technologies.
  - This framework should expose the hardware functionalities directly as APIs or services
  - This car OS should be independent, standardized & interoperable, as well as safe, secure, efficient and easily accessible
- This call has a focus on
  - ***Modular (open-source)*** *building blocks*
  - ***Open architectures*** of the ***SDV middleware and API framework*** for the *vehicle of the future*.
  - ***Holistic engineering framework***

Chips JU RIA proposals *(II Phase to Open)*

- RIA proposal is characterized by
  - The activities have their centre of gravity at **TRL 3-4**
  - Execution normally by an **academy led consortium**
  - Developing **innovative disruptive technologies**
  - Targeting **demonstration of the innovative approach**, clearly addressing relevant societal challenges
  - Demonstrating **value and potential in a realistic lab environment** reproducing the targeted application
  - Having a **deployment plan showing the valorisation for the ECS ecosystem** and the contribution to the Chips JU goals and objectives

Focus Topic Sustainable and Greener Manufacturing *(II Phase to Open)*

- This focus topic concerns the development of a **sustainable and greener semiconductor manufacturing** through the reduction of its environmental footprint with a **focus on materials**. The results of the project are expected to contribute to the following outcomes:

  - Increase the use of **environmentally friendly materials**, chemicals and solvents.
  - **Minimization of waste** and emissions during production and processing
  - Prevention of a future scarcity of some critical materials for SC processing through a **more efficient and cost-effective products** and **electronic waste recycling** in process., including chips and PCBs.

Joint call with Korea *(Closed Call)*

- This joint call for proposals between the Republic of Korea and the EU addresses the topics related to **Heterogeneous integration and neuromorphic computing technologies** for future semiconductor components and systems and intends to set a framework
  - To strengthen the relation between R&I players in both jurisdictions
  - To undertake joint R&I for EU and Korean R&I teams by cooperating in pre-competitive projects on areas which are in the interest of both jurisdictions.
  - To build trust for further cooperation.
- This joint call topic will be co-funded by South Korea (KR) and the European Union (EU)
- This call has very specific conditions. Please conslut the call text in the work programme

EU Funding Rates

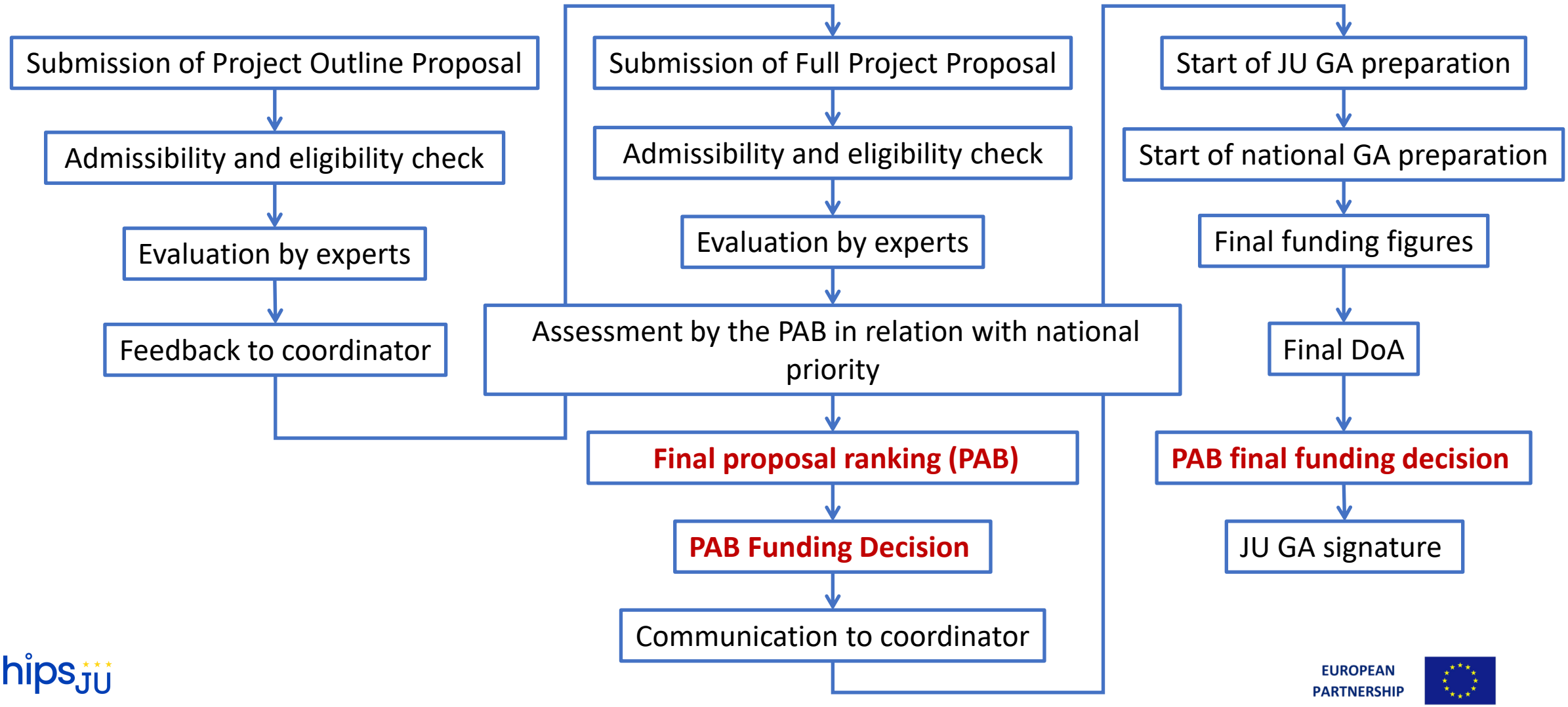
Type of beneficiary	2024-1-IA	2024-1-IA Focus Topics	2024-2-RIA	2024-2-RIA Focus Topic	2024-3-IA
Large Enterprise	20 %	25 %	25 %	25 %	100%
SME	30 %	30 %	35 %	35 %	100%
University/Other (not for profit)	35 %	35 %	35 %	35 %	100%
National Funding	YES	YES	YES	YES	NO

Schedule

Calls 2024-1 and 2024-2	Two stage Call with submission of Project Outline (PO) and Full Proposal (FPP)
Publication date	06 February 2024
Deadline PO Phase	14 May 2024 at 17:00 Brussels Time
Deadline FPP Phase	17 September 2024 at 17:00 Brussels Time
PAB selection	November 2024
Grant preparation	December 2024 to April 2025
Start of the projects	around May 2025

For the Call2024-3, there is no PO phase only an FPP phase with e deadline on 14 May 2024

Proposal Evaluation, Selection, and Grant Agreement Preparation



EUROPEAN PARTNERSHIP

Useful links

Check regularly the call information under the CHIPS website:

https://www.chips-ju.europa.eu/

Address eventual questions related to the calls to:

calls@chips-ju.europa.eu

Consult the sections on the 2024 calls in the:

Chips JU Work Programme

CHIPS JU INITIATIVE CALLS

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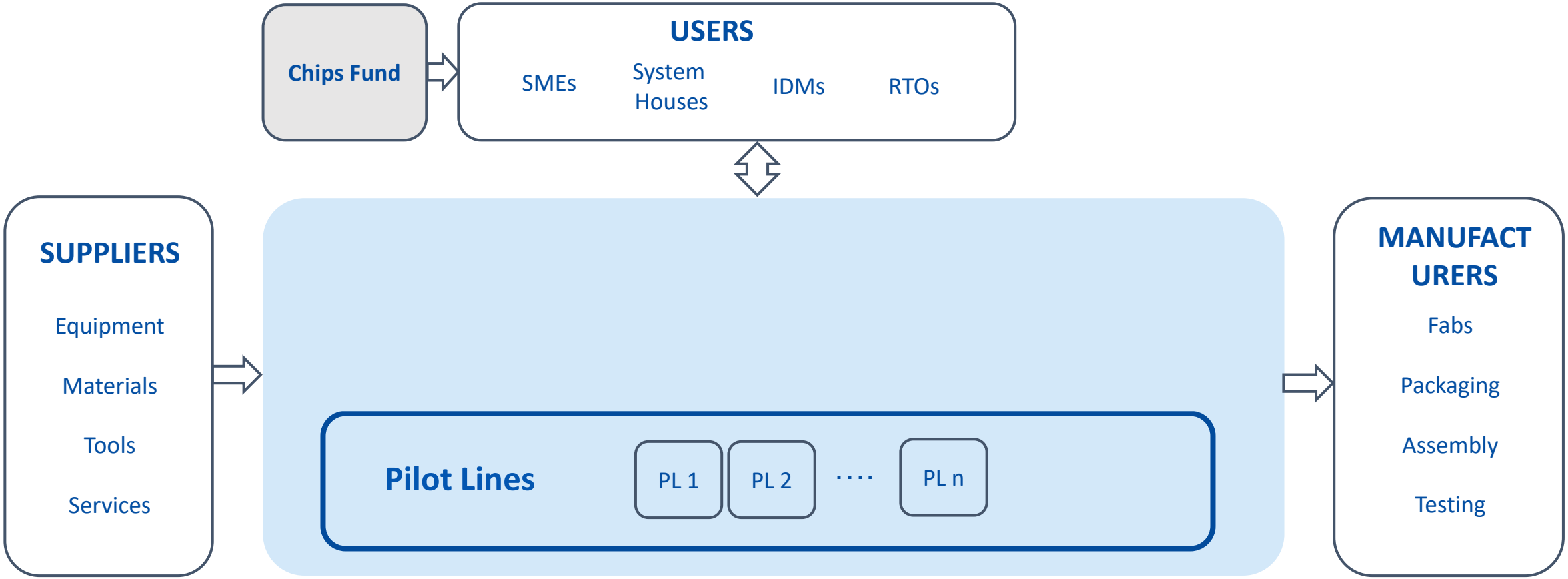
27/09/2024

EUROPEAN PARTNERSHIP

Chips for Europe Initiative

From lab to fab



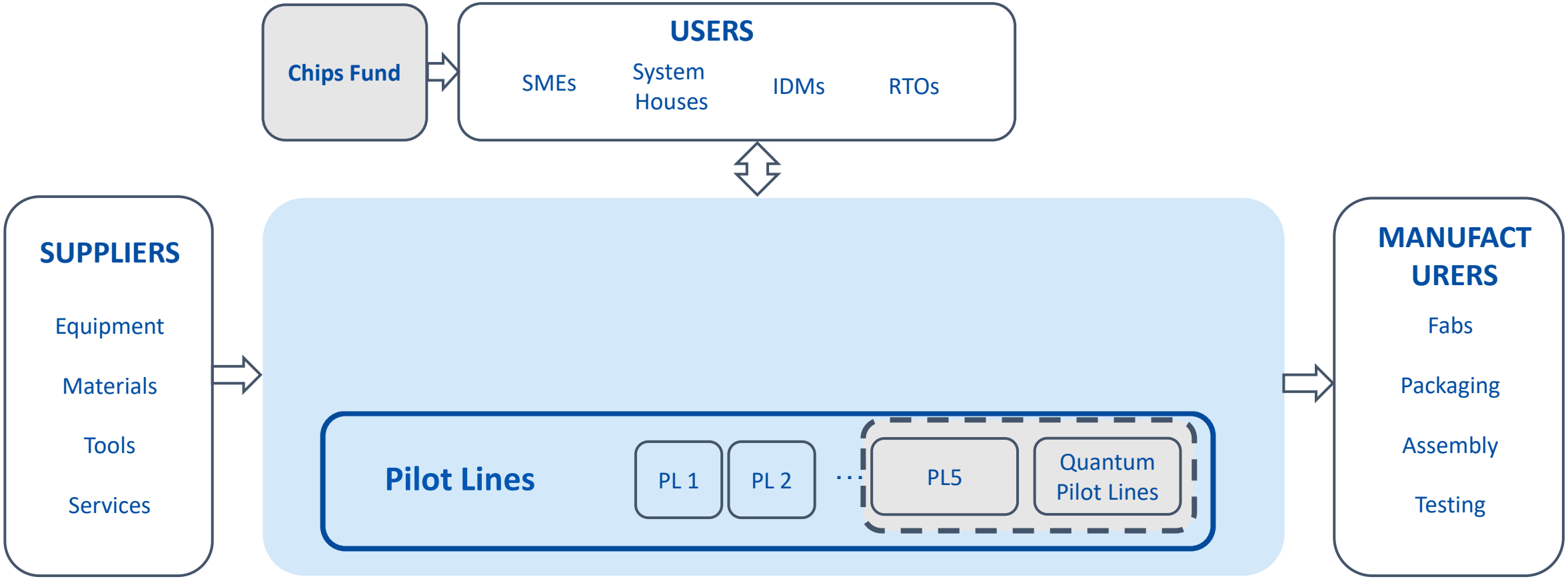
2. Chips JU Calls 2023- Initiative

Four Calls for Pilot Lines (CPL)

Pilot line	EU Budget
Pilot line on advanced sub 2nm leading-edge system on chip technology	700 million Euro
Pilot line on advanced Fully Depleted Silicon On Insulator technologies targeting 7nm	420 million Euro
Pilot line on advanced Packaging and Heterogenous Integration	370 million Euro
Pilot line on advanced semiconductor devices based on Wide Bandgap materials	180 million Euro

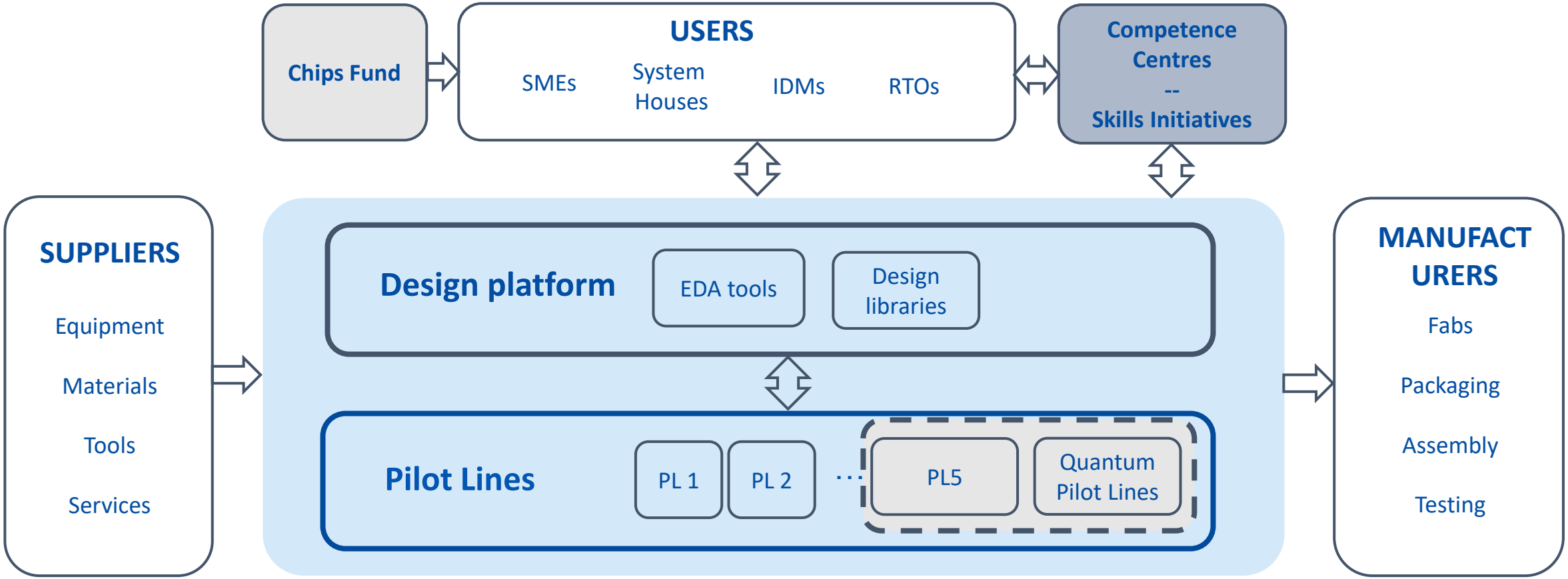
Chips for Europe Initiative

From lab to fab



Chips for Europe Initiative

From lab to fab



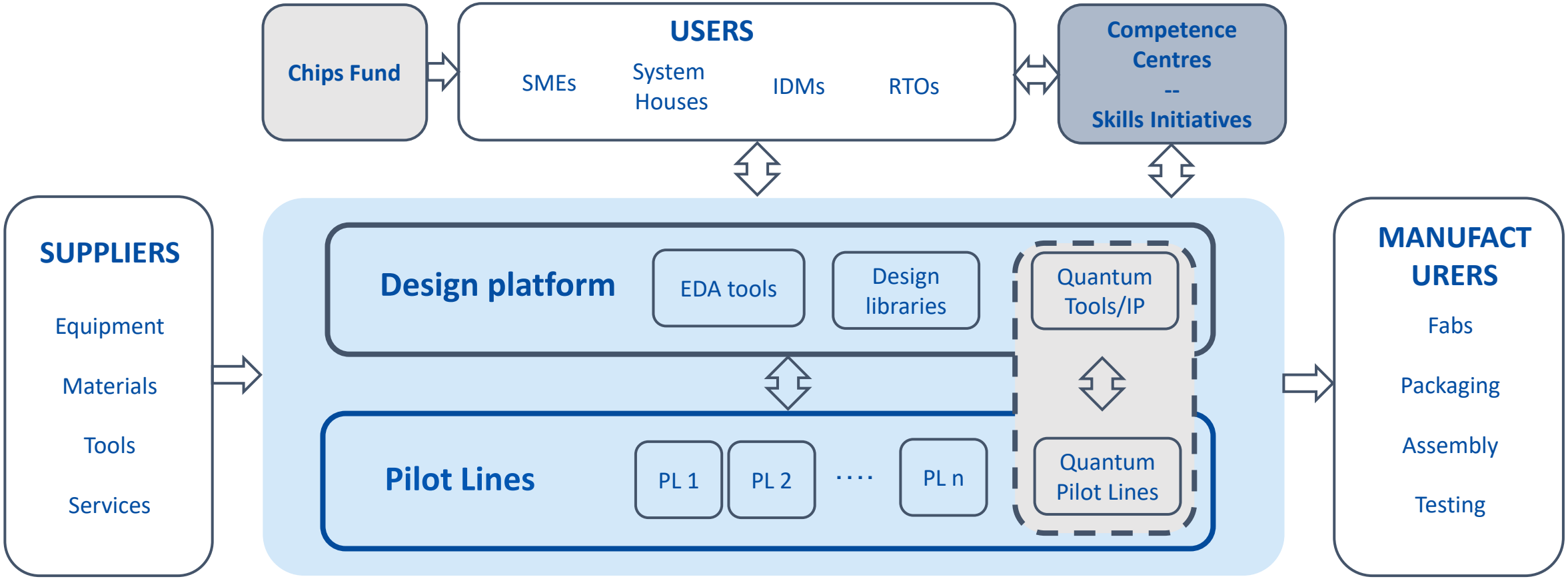
EUROPEAN PARTNERSHIP

2. Chips JU Calls 2024- Initiative

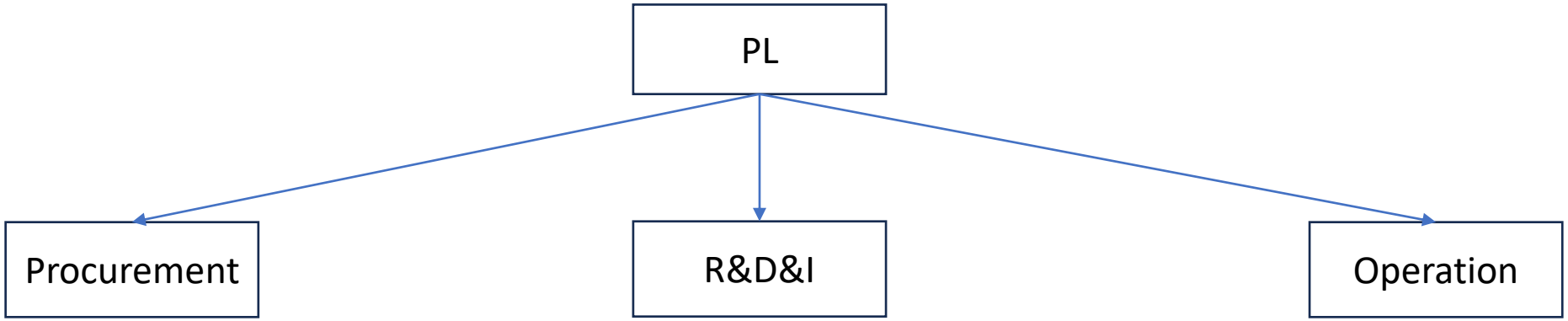
Pilot line	EU Budget
Competence Centres (Grant under Digital Europe)	116 million Euro
Competence Centre Network (CSA under Digital Europe)	4 million Euro
Design Platform	25 million Euro
Call For Pilot Line on Advanced Photonic Integrated Circuits	190 million Euro
Action on quantum technologies pilot (FPA)	0

Chips for Europe Initiative

From lab to fab



Chips JU Pilot lines

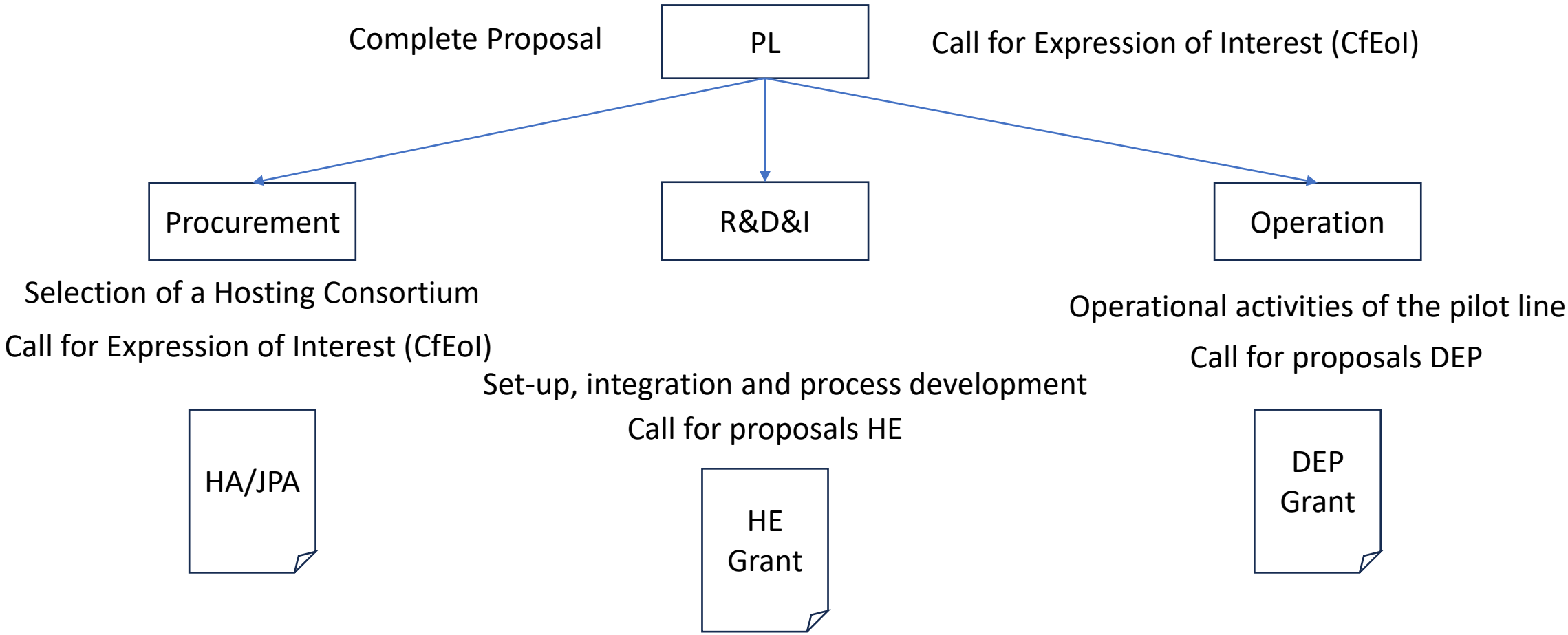


Facilities
(existing and to be build)
Equipment
(existing and to be purchased)
… … …

Materials
Recipes
Methods
Technology modules,
Metrology,
Control systems
… … …

Offered technologies
Services
Capacity
Access
… … …

Chips JU PL Calls and Grants



Competence Centres

EU support for at least one centre per Member State

Co-investment with Member States and Regions

Supporting industry and public services

Access to design platform and pilot lines

Focus on Semiconductors Skills

A strong European network of Competence Centres

Competence Centres

Main services:

- Have specialised areas of expertise in certain technology, domain, or activities (**specialisation**)
- Facilitate effective use of capacities and facilities, including access to **design platform** and **pilot lines**
- Support interested stakeholders in developing semiconductor solutions (**technology transfer**)
- Address **skills shortage** by offering (access to) **training** on semiconductors, including workforce upskilling and reskilling
- Match user needs with available expertise in network of competence centres and act as **access point to the network**
- **Promote Chips Fund** and facilitate access to venture capital
- **Awareness raising, promoting services, promoting success stories**

Entities Forming Competence Centres and Users

- **Competence centre**: single organisation or coordinated group of organisations with complementary expertise, established with non-profit objective, aiming to promote the use of semiconductor technologies

- Competence centers can be built on established entities in the field or can be set up from scratch

- **Users**: companies, in particular local/national SMEs and startups, RTOs, academic institutions, public authorities

Funding Model

- European **network of competence centres** in semiconductors, system integration and design shall be established
- Participating States may decide not to nominate any candidate entity to become a competence centre in its territory, or to nominate together with other countries (cross-border competence centre)
- Participating States are expected to **co-finance** their national competence centres **on a 50-50 basis**
- EU funding: **max EUR 1 million per year, per country, for a 4-year period**, provided that same or higher national co-financing is available

Service Offerings

- Access to competence centres' services shall be granted on an open, transparent and non-discriminatory basis
- Services to **SMEs** and **public sector** organisations: **free** or against **reduced prices**
- **Larger companies**: against **market price** or **actual costs**

Network of Chips Competence Centres

- The European semiconductor ecosystem will be strengthened through an effective network of Chips Competence Centres (Chips CCs) supporting the adoption and use of semiconductor technologies, in particular by SMEs, and taking into account the specific needs of the local, regional and/or national ecosystem(s)
- The coordinated network will facilitate access to pilot lines and the European virtual design platform and knowledge transfer within the Chips CCs
- The European network of Chips Competence Centres will be embedded in the European semiconductor ecosystem with strong links to other European initiatives, for example, in the area of training

Coordination and Support Action of CCC

- To maximize networking between existing European points of semiconductor knowledge and expertise Chips JU is launching a call for Coordination and Support Action
- This action will provide a single focal point at European level, which will be responsible for the support of the Chips Competence Centres,
- It will ensure:
  - Effective coordination and exchange of best practices and information among the network of Chips CCs;
  - Facilitated access to services and training offered at national or regional level to interested Chips CCs and other potential users (from industry, academia or public sector);
  - Maximised visibility and outreach of Chips CCs, in particular to SMEs and industry;
  - Improved coordination and increased availability of training activities on semiconductor technologies across Chips CCs and within the European semiconductor ecosystem;
- In order to accomplish these objectives, the selected consortium should also establish effective cooperation with other European initiatives, in particular regarding skills and training in semiconductors.

Pilot Line on Advanced Photonic Integrated Circuits

- To address these challenges Chips JU is launching a call for dedicated pilot line for Photonic Integrated Circuits within Europe.
- This initiative will focus on advancing PIC technologies beyond the current state-of-the-art crucial for tapping into new application areas such as biomedical imaging, quantum computing, and environmental sensing.
- The proposed pilot line will serve as a critical infrastructure for bridging the gap between laboratory research and industrial-scale production, facilitating the development of reliable, scalable, and cost-effective PIC solutions.
- Such a pilot line will not only enhance Europe's competitive edge in a key technological domain but also contribute significantly to the continent's economic resilience and strategic autonomy in critical technologies.

Semiconductor Circuit Design

- Semiconductor circuit design is the process of creating integrated circuits (ICs) and system-on-chips (SoCs) by defining the functionalities and characteristics of chips, capturing a substantial portion of the added value within the semiconductor value chain.
- The trend is moving towards more complex, application-specific, highly integrated semiconductors, making cutting-edge design crucial for competitiveness and differentiation in a wide range of applications.
- In this context, fabless companies are well-positioned to drive technological advancements and meet the needs of diverse applications
- The Chips Act underscores the strategic importance of fostering chip design growth in Europe to enhance the competitiveness of the Union’s semiconductor industry and to strengthen the Union's resilience in semiconductor technologies, including promoting the growth of fabless companies focused on leading-edge technologies.
- This is especially pertinent given that the European share of global fabless semiconductor companies’ revenues has shrunk to critically low levels (currently around 1%)
- It is strategically important to foster chip design growth in Europe to enhance the competitiveness of the Union’s semiconductor industry.
- A critical mass of fabless companies is also key to generate further demand that would justify increased investment in semiconductor manufacturing capacity in Europe.

Design Platform

- To address these challenges Chips JU is launching a call for a Design Platform
- The Design Platform shall focus on nurturing emerging companies in the sector. The Design Platform is at the heart of the Chips for Europe Initiative, it is envisaged as a key instrument to foster the development of a strong design ecosystem in the Union, by creating a pipeline of highly innovative European fabless companies, focusing particularly on the growth of start-ups and SMEs.
- The primary objectives of the platform are to cultivate a robust chip-design ecosystem in Europe and to ensure that start-ups and SMEs have access to top-tier tools and support services comparable to those more easily accessible to large enterprises.
- This platform, as a unified European infrastructure combined with comprehensive user support services, aims to democratise chip design in Europe by facilitating access, for all eligible users, to advanced tools and resources, irrespective of their size.
- To this end, the Design Platform shall encompass a combination of a cloud-based infrastructure together with a number of dedicated design and other relevant services and activities
- The main target users of the Design Platform shall be commercial entities, particularly start-ups and SMEs, for the purpose of pre-competitive activities such as research, development and innovation up to experimentation and tape-out.
- Such entities are then expected to engage in regular commercial contractual agreement with Electronic Design and Automation tool vendors outside of the Design Platform upon maturity.
- Complementary support to that already provided by EUROPRACTICE for academia and research institutes can be considered.

CHIPS JU CALLS 2025

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27/09/2024

EUROPEAN PARTNERSHIP

Chips JU None Initiative Calls 2025

Action	Title	Maximum JU Funding (M€)
HORIZON-Chips 2025-1-IA-T1	Global IA call according to SRIA 2025	
HORIZON-Chips 2025-1-IA-T2	Focus topic	
HORIZON-Chips 2025-1-IA-T3	Focus topic	
HORIZON- Chips 2025-2-RIA-T1	Global RIA call according to SRIA 2025	
HORIZON- Chips 2025-2-RIA-T2	Focus topic	
HORIZON- Chips 2025-3-RIA	Joint call with Japan	

2. Chips JU Calls 2025- Initiative

Pilot line	EU Budget
Further actions on the DP (DETs; Open source EDA tools; Support for SMEs and startups)	
Further actions on the CC	
Action on quantum technologies pilot (SGA)	
Lab-to-Fab	
Europractice	
Pilot line ?	

Planning Calls 2024 Non-Initiative